What is claimed is:

1. A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film,

the end portions in the gate length direction of said gate insulating film being positioned inwardly from the respective end portions on the source side and on the drain side of said gate electrode, and said end portions of said gate insulating film being positioned in a region in which said gate electrode overlaps with a source region and a drain region in plan configuration.

2. A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film, and the end portions in the gate length direction thereof being positioned inwardly from the respective end portions on

the source side and on the drain side of said gate electrode, and

a source region and a drain region of said field effect transistor extending into the underlying portion of said gate insulating film.

3. The semiconductor device according to claim 1, wherein an insulating film having a lower dielectric constant than that of said gate insulating film is provided laterally of the end portions in the gate length direction of said gate insulating film, and on said semiconductor substrate.

4. The semiconductor device according to claim 1, wherein the end portions in the gate length direction of said gate insulating film are positioned inwardly from the respective end portions on the source side and on the drain side of said gate electrode by 15 nm to 25 nm, respectively.

5. The semiconductor device according to claim 1, wherein said gate insulating film is an oxide, an oxynitride, or a silicate compound of at least one metal selected from the group consisting of titanium, tantalum, hafnium, zirconium, aluminium, lanthanum, and strontium.

6. The semiconductor device according to claim 1, wherein said gate insulating film has a laminated structure of a layer comprising an oxide of at least one metal selected from the group consisting of titanium, tantalum, hafnium, zirconium, aluminium, lanthanum, and strontium, and

a layer comprising a silicate compound of said metal.

7. The semiconductor device according to claim 1, wherein said source region and said drain region do not contain the metal contained in said insulating film, or contain said metal in a concentration of 10^{11} atom/cm^2 or less.

8. The semiconductor device according to claim 1, wherein said gate electrode is a metal selected from at least one selected from the group consisting of tungsten, titanium, and molybdenum, or a nitride thereof or a silicide thereof.

9. A method for manufacturing a semiconductor device, comprising the steps of:

forming an insulating film having a higher dielectric constant than that of a silicon dioxide film on a semiconductor substrate, and forming a conductive film on said insulating film;

processing said conductive film into a gate electrode;

removing said insulating film having a higher dielectric constant so that the part underlying said gate electrode is left, and the end portions of the residual part are positioned inwardly of the end portion on the side on which a source region is to be formed and the end portion on the side on which a drain region is to be formed of said gate electrode, and thereby allowing said residual part to serve as a gate insulating film;

forming a second insulating film having a lower dielectric constant than that of said gate insulating film at

least laterally in the gate length direction of said gate electrode, and on said semiconductor substrate; and

implanting a dopant into said substrate through said second insulating film by an ion implantation method to form said source region and said drain region, and allowing said source region and said drain region to extend into the underlying portion of said gate insulating film.

10. The method for manufacturing a semiconductor device according to claim 9, wherein said insulating film having a higher dielectric constant is formed in amorphous state, and the removal of said insulating film having a higher dielectric constant is performed by removing a part of said film by dry etching, and then further by wet etching.

11. The method for manufacturing a semiconductor device according to claim 10, wherein said insulating film having a higher dielectric constant is crystallized after said wet etching.

12. The method for manufacturing a semiconductor device according to claim 9, wherein the implantation of said dopant is performed by an oblique ion implantation method.

13. The method for manufacturing a semiconductor device according to claim 9, wherein the removal of said insulating film having a higher dielectric constant is performed such that the end portions of said residual part are positioned inwardly from the respective end portions on the source region side and

on the drain region side of said gate electrode by 15 nm to 25 nm, respectively.

14. The method for manufacturing a semiconductor device according to claim 9, wherein said gate insulating film is an oxide, an oxynitride, or a silicate compound of at least one metal selected from the group consisting of titanium, tantalum, hafnium, zirconium, aluminium, lanthanum, and strontium.

15. The method for manufacturing a semiconductor device according to claim 9, wherein said gate electrode is a metal selected from at least one selected from the group consisting of tungsten, titanium, and molybdenum, or a nitride thereof or a silicide thereof.

16. The method for manufacturing a semiconductor device according to claim 9, wherein said gate electrode comprises a polysilicon, and a plurality of said gate electrodes have mutually different work functions because the substance used for said ion implantation differs from one gate electrode to another.

17. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first insulating film having a higher dielectric constant than that of a silicon dioxide film on a semiconductor substrate, forming a second insulating film having a higher dielectric constant than that of said first insulating film on said first insulating film, and forming a

conductive film on said second insulating film;

processing said conductive film into a gate electrode;

removing said second insulating film so that the part underlying said gate electrode is left, and the end portions of the residual part are positioned inwardly of the end portion on the side on which a source region is to be formed and the end portion on the side on which a drain region is to be formed of said gate electrode, and thereby allowing said residual part to serve as a gate insulating film; and

implanting a dopant into said substrate through said first insulating film by an ion implantation method to form said source region and said drain region, and allowing said source region and said drain region to extend into the underlying portion of said gate insulating film.

18. The method for manufacturing a semiconductor device according to claim 17, wherein said gate insulating film is an oxide or an oxynitride of at least one metal selected from the group consisting of titanium, tantalum, hafnium, zirconium, aluminium, lanthanum, and strontium, and

said second insulating film is a silicate compound.

19. The method for manufacturing a semiconductor device according to claim 17, wherein said gate electrode is a metal selected from at least one selected from the group consisting of tungsten, titanium, and molybdenum, or a nitride thereof or a silicide thereof.

20. The method for manufacturing a semiconductor device according to claim 17, wherein the removal of said second insulating film is performed such that the end portions of said residual part are positioned inwardly from the respective end portions on the source region side and on the drain region side of said gate electrode by 15 nm to 25 nm, respectively.